IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Atty. Dkt. No. 5298-02501
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Inventor(s):
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Title: PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT

§

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Derrick Brown

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir/Madam:

The captioned application is a continuation application pursuant to 37 C.F.R. § 1.53(b) from prior application 09/143,723 filed August 31, 1998. Prior to initial examination of the captioned matter, please amend the case as follows:

In the Specification:

Please amend the specification as follows. A "marked-up" version of these amendments is included in **Attachment A**.

Please replace the paragraph on pg. 4, line 13 - pg. 5, line 3 with the following:

Unfortunately, the topological surface of the interconnect level is not absent of elevational disparity. That is, the upper surface of interconnect 38 includes a recessed area 42 that extends below a substantially planar upper surface 44 of interlevel dielectric 20. Recessed area 42 may result from a phenomena known as the "dishing" effect. Dishing naturally results